`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 07/12/2022 10:49:28 AM

// Design Name:

// Module Name: palu\_unit\_tb

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

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//////////////////////////////////////////////////////////////////////////////////

module palu\_unit\_tb;

reg [7:0] a =8'b0;

reg [7:0] b = 8'b0;

reg [1:0] s = 2'd0;

wire [7:0] f;

wire ovf;

eightbit\_palu UUT(

.a(a),

.b(b),

.s(s),

.f(f),

.ovf(ovf)

);

initial begin

s=2'd0; a=8'd0;b=8'd0;

#100;

a=-8'd12; b=-8'd34;

#100;

a=8'd100; b=8'd100;

#100;

s=2'd1; a=8'd1; b=8'd1;

#100;

a=-8'd12; b=-8'd12;

#100;

a=8'd100; b=8'd100;

#100;

s=2'd2; a=8'd1; b=8'd1;

#100;

a=8'd1; b=8'd3;

#100;

a=-8'd4; b=-8'd5;

#100;

s=2'd3; a=8'd1; b=8'd1;

#100;

a=8'd12; b=-8'd16;

#100;

a=-8'd2; b=-8'd6;

end

endmodule